



## VTG Interface Adapter

# VIA-LVDS

### Digital Interface Adapters for Flat Panel Displays

The VIA-LVDS, VTG Interface Adapter, is a high-speed digital display interface for converting 24 or 48 bits of parallel pixel-data, clock & sync signals to LVDS differential serial signal for LDI and open LDI output interfaces.

### Total Flexibility for all your needs

Every VIA comes equipped with floppy-disk, containing appropriate .vtm file for driving the VIA. Interface parameters and their preset values are specified in .vtm file. The user adjustable parameters are shown in the Edit TIMING Menu. These values can be SAVED in TIMING file. If the VIA-parameters should NOT be SAVED, use File-Configure: Silent Mode during SAVE.

This .vtm file should be copied to the Specified path in File-Configure menu VIA files (PM files). All .vtm files for different Vtg Interface Adapters can be SAVED here, when their names are different. Filename std0821.vtm consists of first three letters (std) then four numbers (0821) and .vtm. This last number (this case) is related to the VIA address on the VIA pcb ADDRESS jumpers. If the last number in the filename is changed, also the four jumper setting must be changed accordingly.

If there is no appropriate .vtm file and VIA ADDRESS jumpers pair available, Edit TIMING Menu shows:

Cannot open VTM file.

If TIMING file does not have corresponding parameters with the correct .vtm file Edit TIMING Menu shows:

PMID matching failure.

It is possible to see the VIA ADDRESS jumpers setting number in the TIMING Menu, Clock section.

All this enables this kind of standard interfacing protocol to different kinds of Display Interfaces now and in the future.

### The VIA Advantage

- Full ATE support.
- DDC Support.
- Lower Cost, when standards change all you need to change is the adapter, not a complete generator!

### Full Software Support

- Interface controlling and adjusting is software controlled via the UNIGRAF Windows User Interface.
- Drivers for Win95, Win98 and NT 16 and 32 bit DLLs.

### The right VIA for your application

Due to the changing markets and standards the VTG-1108 and VTG Interface Adapters are the preferred choice. There are VIA's available for LVDS, TMDS, Parallel-TTL and RGB interfaces.

# UNIGRAF

## VIA - LVDS

### Input signals

PixelClock 112MHz MAX  
Pixel Frequency 224 MHz MAX  
DATA 48 bits = 2 x 24bit Pixels  
Blank=DE=DataEnable  
Hsync, Vsync  
VIA-ControlBus D0..D8  
PbRdL, PbWrL, PbResL  
DDC: SCL, SDA, +5 V DDC  
Vcc +5 V, +12 V from PC

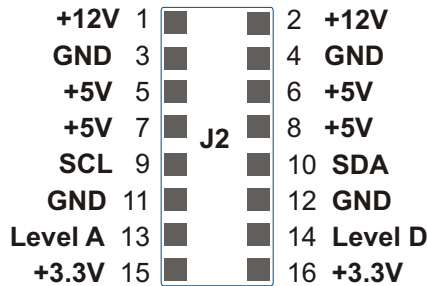
### Input connector DHP100 DsubHalfPith

GND	-----	1	PIN	51	-----	GND
XR0	-----	2	PIN	52	-----	YR0
XR1	-----	3	PIN	53	-----	YR1
GND	-----	4	PIN	54	-----	GND
XR2	-----	5	PIN	55	-----	YR2
XR3	-----	6	PIN	56	-----	YR3
GND	-----	7	PIN	57	-----	GND
XR4	-----	8	PIN	58	-----	YR4
XR5	-----	9	PIN	59	-----	YR5
GND	-----	10	PIN	60	-----	GND
XR6	-----	11	PIN	61	-----	YR6
XR7	-----	12	PIN	62	-----	YR7
GND	-----	13	PIN	63	-----	GND
XG0	-----	14	PIN	64	-----	YG0
XG1	-----	15	PIN	65	-----	YG1
GND	-----	16	PIN	66	-----	GND
XG2	-----	17	PIN	67	-----	YG2
XG3	-----	18	PIN	68	-----	YG3
GND	-----	19	PIN	69	-----	GND
XG4	-----	20	PIN	70	-----	YG4
XG5	-----	21	PIN	71	-----	YG5
GND	-----	22	PIN	72	-----	GND
XG6	-----	23	PIN	73	-----	YG6
XG7	-----	24	PIN	74	-----	YG7
GND	-----	25	PIN	75	-----	GND
XB0	-----	26	PIN	76	-----	YB0
XB1	-----	27	PIN	77	-----	YB1
GND	-----	28	PIN	78	-----	GND
XB2	-----	29	PIN	79	-----	YB2
XB3	-----	30	PIN	80	-----	YB3
GND	-----	31	PIN	81	-----	GND
XB4	-----	32	PIN	82	-----	YB4
XB5	-----	33	PIN	83	-----	YB5
GND	-----	34	PIN	84	-----	GND
XB6	-----	35	PIN	85	-----	YB6
XB7	-----	36	PIN	86	-----	YB7
GND	-----	37	PIN	87	-----	GND
PCLK	-----	38	PIN	88	-----	PbRdL
GND	-----	39	PIN	89	-----	PbWrL
Blank	-----	40	PIN	90	-----	D0
HSync	-----	41	PIN	91	-----	D1
VSynC	-----	42	PIN	92	-----	D2
NC	-----	43	PIN	93	-----	D3
NC	-----	44	PIN	94	-----	D4
GND	-----	45	PIN	95	-----	D5
SCL	-----	46	PIN	96	-----	D6
SDA	-----	47	PIN	97	-----	D7
+5DDC	-----	48	PIN	98	-----	PbResL
Vcc+5	-----	49	PIN	99	-----	GND
Vcc+12V	-----	50	PIN	100	-----	Vcc+12V

### VIA-LVDS jumpers

**J1:** VIA address (PMID) JUMPERS  
Defines the last address digit in VIA address  
ref: stdxxx(J1(H)).vtm

**J2:** EXTRA output connector inside VIA for backlighting and display electronics



**J3:** LDI Pin 19 output select

1-2 +5 V  
2-3 GND  
- NC

**J4:** LDI Pin 7 output select

1-2 SCL  
2-3 GND  
- NC

**J5:** LDI Pin 20 output select

1-2 SDA  
2-3 GND  
- NC

**J6:** Open LDI Pin 11 output select

ON +5V  
- NC

**J7:** Open LDI Pin 13 output select

ON +5V  
- NC

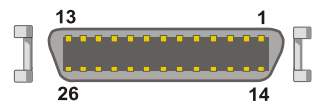
**J8 & J9:** LDI Pin 1&14 output select

ON - ON pin 1 CLK2- pin14 CLK2+  
- NC

**J10:** External power input connector for 12V DC (MAX 3A)  
Type of connector: ROKA 520 2550

### LDI output Interface

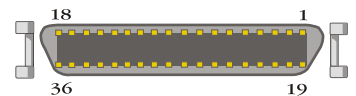
MDR26 connector  
(Configured using jumpers)



1. J8/2	14. J9/2
2. GND	15. CTX0-
3. CTX0+	16. CTX1-
4. CTX1+	17. CTX2-
5. CTX2+	18. CTXC-
6. CTXC+	19. J3/2
7. J4/2	20. J5/2
8. GND	21. CTX3-
9. CTX3+	22. CTX4-
10. CTX4+	23. CTX5-
11. CTX5+	24. CTX6-
12. CTX6+	25. CTX7-
13. CTX7+	26. GND

### OpenLDI output Interface

MDR36 connector  
(Configured using jumpers)



1. BTX0-	19. BTX0+
2. BTX1-	20. BTX1+
3. BTX2-	21. BTX2+
4. BTXC-	22. BTXC+
5. BTX3-	23. BTX3+
6. GND	24. NC
7. NC	25. NC
8. NC	26. NC
9. NC	27. GND
10. SCL	28. SDA
11. J6/2	29. GND
12. YJ2/1	30. YJ2/2
13. J7/2	31. GND
14. BTX4-	32. BTX4+
15. BTX5-	33. BTX5+
16. BTX6-	34. BTX6+
17. BTX7-	35. BTX7+
18. CLK2M	36. CLK2P

National Semiconductor  
DS90C387  
LVDS chips inside

### Software adjustment parameters

<b>Pd LDI (= Power Down)</b>	0=LVDS output Power DOWN 1=LVDS output Power ON
<b>Pd open LDI (= Power Down)</b>	0=LVDS output Power DOWN 1=LVDS output Power ON
<b>DC balance</b>	Conventional LVDS 0=Not Balanced Advanced LVDS Feature 1=DCbalanced
<b>LDI Pre Emphasis</b>	Output LVDS peaking for Longer cables and difficult loads
<b>Open LDI Pre Emphasis</b>	Output LVDS peaking for Longer cables and difficult loads
<b>Level A</b>	Level adjustment for Output DC voltage A in J2 pin 13
<b>Level D</b>	Level adjustment for Output DC voltage D in J2 pin 14

ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE